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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Terminal equipments – General

Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels

ITU-T Recommendation G.704

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION G.704

SYNCHRONOUS FRAME STRUCTURES USED AT 1544, 6312, 2048, 8448 AND 44 736 kbit/s HIERARCHICAL LEVELS

Summary

This Recommendation gives functional characteristics of interfaces associated with:

– network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs; and

– PCM multiplexing equipment.

Clause 2 deals with basic frame structures, including details of frame length, frame alignment signals, Cyclic Redundancy Check (CRC) procedures and other basic information.

Clauses 3 to 6 contain more specific information about how certain channels at 64 kbit/s and at other bit rates are accommodated within the basic frame structures described in clause 2.

Source

ITU-T Recommendation G.704 was revised by ITU-T Study Group 15 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 13th of October 1998.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation the term *recognized operating agency (ROA)* includes any individual, company, corporation or governmental organization that operates a public correspondence service. The terms *Administration, ROA* and *public correspondence* are defined in the *Constitution of the ITU (Geneva, 1992)*.

INTELLECTUAL PROPERTY RIGHTS

The ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. The ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, the ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Recommendation G.704

SYNCHRONOUS FRAME STRUCTURES USED AT 1544, 6312, 2048, 8448 AND 44 736 kbit/s HIERARCHICAL LEVELS

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988; revised in 1990, 1995 and 1998)

1 Scope

This Recommendation gives functional characteristics of interfaces associated with:

– network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs; and

– PCM multiplexing equipment.

Clause 2 deals with basic frame structures, including details of frame length, frame alignment signals, Cyclic Redundancy Check (CRC) procedures and other basic information.

Clauses 3 to 6 contain more specific information about how certain channels at 64 kbit/s and at other bit rates are accommodated within the basic frame structures described in clause 2.

Electrical characteristics for these interfaces are defined in Recommendation G.703.

NOTE 1 – This Recommendation does not necessarily apply to those cases where the signals that cross the interfaces are devoted to non-switched connections, such as those for the transport of encoded wideband signals (e.g. broadcast TV signals or multiplexed sound-program signals which need not be individually routed via the ISDN). See also Annex A/G.702.

NOTE 2 – The frame structures recommended in this Recommendation do not apply to certain maintenance signals, such as the all 1s signals transmitted during fault conditions or other signals transmitted during out-of-service conditions.

NOTE 3 – Frame structures associated with digital multiplexing equipments using justification are covered in each corresponding equipment Recommendation.

NOTE 4 – Inclusion of channel structures at bit rates other than 64 kbit/s is a matter for further study. Recommendations G.761 and G.763 dealing with the characteristics of PCM/ADPCM transcoding equipment contain information about channel structures at 32 kbit/s. The more general use of those particular structures is a subject of further study.

2 Basic frame structures

2.1 Basic frame structure at 1544 kbit/s

2.1.1 Frame length

193 bits, numbered 1 to 193. The frame repetition rate is 8000 Hz.

2.1.2 F-bit

The first bit of a frame is designated an F-bit, and is used for such purposes as frame alignment, performance monitoring and providing a data link.

2.1.3 Allocation of F-bit

Two alternative methods as given in Tables 1 and 3 for allocation of F-bits are recommended.

2.1.3.1 Method 1: 24-frame multiframe

Allocation of the F-bit to the multiframe alignment signal, the CRC check bits and the data link is given in Table 1.

Table 1/G.704 – Multiframe structure for the 24-frame multiframe

Frame number within multiframe	F-bit				Bit number(s) in each channel time slot		Signalling channel designation[a]
	Bit number within multiframe	Assignments					
		FAS	DL	CRC	For character signal[a]	For signalling[a]	
1	1	–	m	–	1-8	–	
2	194	–	–	e_1	1-8	–	
3	387	–	m	–	1-8	–	
4	580	0	–	–	1-8	–	
5	773	–	m	–	1-8	–	
6	966	–	–	e_2	1-7	8	A
7	1159	–	m	–	1-8	–	
8	1352	0	–	–	1-8	–	
9	1545	–	m	–	1-8	–	
10	1738	–	–	e_3	1-8	–	
11	1931	–	m	–	1-8	–	
12	2124	1	–	–	1-7	8	B
13	2317	–	m	–	1-8	–	
14	2510	–	–	e_4	1-8	–	
15	2703	–	m	–	1-8	–	
16	2896	0	–	–	1-8	–	
17	3089	–	m	–	1-8	–	
18	3282	–	–	e_5	1-7	8	C
19	3475	–	m	–	1-8	–	
20	3668	1	–	–	1-8	–	
21	3861	–	m	–	1-8	–	
22	4054	–	–	e_6	1-8	–	
23	4247	–	m	–	1-8	–	
24	4440	1	–	–	1-7	8	D

FAS Frame alignment signal (... 001011 ...)

DL 4 kbit/s data link (message bits m)

CRC CRC-6 block check field (check bits e_1 to e_6)

[a] Only applicable in the case of channel associated signalling (see 3.1.3.2).

2.1.3.1.1 Multiframe alignment signal

The F-bit of every fourth frame forms the pattern 001011 ... 001011. This multiframe alignment signal is used to identify where each particular frame is located within the multiframe in order to extract the cyclic redundancy check code, CRC-6, and the data link information, as well as to identify those frames that contain signalling (frames 6, 12, 18 and 24), if channel associated signalling is used.

2.1.3.1.2 Cyclic Redundancy Check (CRC)

The CRC-6 is a method of performance monitoring that is contained within the F-bit position of frames 2, 6, 10, 14 18 and 22 of every multiframe (see Table 1).

The CRC-6 message block check bits e_1, e_2, e_3, e_4, e_5, and e_6 are contained within multiframe bits 194, 966, 1738, 2510, 3282 and 4054 respectively, as shown in Table 1. The CRC-6 Message Block (CMB) is a sequence of 4632 serial bits that is coincident with a multiframe. By definition, CMB N begins at bit position 1 of multiframe N and ends at bit position 4632 of multiframe N. The first transmitted CRC bit of a multiframe is the most significant bit of the CMB polynomial.

In calculating the CRC-6 bits, the F-bits are replaced by binary 1s. All information in the other bit positions will be identical to the information in the corresponding multiframe bit positions.

The check-bit sequence e_1 through e_6 transmitted in multiframe $N + 1$, is the remainder after multiplication by x^6 and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_6) is the least significant bit of the remainder. Each multiframe contains the CRC-6 check bits generated for the preceding CMB.

At the receiver, the received CMB, with each F-bit having first been replaced by a binary 1, is acted upon by the multiplication/division process described above. The resulting remainder is compared on a bit-by-bit basis, with the CRC-6 check bits contained in the subsequently received multiframe. The compared check bits will be identical in the absence of transmission errors.

2.1.3.1.3 4 kbit/s data link

Beginning with frame 1 of the multiframe (see Table 1), the first bit of every other frame is part of the 4 kbit/s data link. This data link provides a communication path between primary hierarchical level terminals. In prioritized order the data link will contain priority operations messages, other maintenance or operations messages, periodic terminal performance reports, or an idle data link sequence.

- Both categories of operations messages are transmitted in the form of 16-bit sequences of the form $11111110P_1P_2P_3P_4P_5P_60$, where the particular message is coded by the six bits P_1 through P_6, permitting up to 64 distinct messages. Designated sequences and their functional uses are listed in Table 2. Use of sequences not shown in the table is for further study.
- Periodic terminal performance reports are formatted using the unnumbered, unacknowledged frame option of Q.921/LAPD, as described in 2.1.3.1.3.3. Transmission of any of the assigned 16-bit sequences terminates any processing of a (lower priority) performance report that might be in progress, as seven or more consecutive ones are recognized in Recommendation Q.921 as an abort command.
- The idle data link sequence is a continuous repetition of the pattern 01111110.
- The transmission of Loss of Frame Alignment (LFA) – also called Remote Alarm Indication (RAI) – and idle data link sequence in m-bits is mandatory. The other use of m-bits is optional, but when a function other than mandatory functions is used, the specification described here should be applied to guarantee the interworking of terminals.

NOTE – Some functions, such as PRM, are mandatory in some national standard.

Table 2/G.704 – Assigned operations data link messages

Priority Messages	
Function	Codeword
LFA (also called RAI)	11111111 00000000
Loopback Retention	11111111 01010100
Other Operation Messages	
Category	
Function	Codeword
Loopbacks:	
Customer Installation Type A Operate	11111111 01110000
Customer Installation Type A Release	11111111 00011100
Customer Installation Type B Operate	11111111 00000100
Customer Installation Type C Operate	11111111 01110100
Payload Operate	11111111 00101000
Payload Release	11111111 01001100
Network Type A Operate	11111111 01001000
Universal Release	11111111 00100100
Protection switching:	
Operate Line 1	11111111 01000010
Operate Line 2	11111111 00100010
Operate Line 3	11111111 01100010
Operate Line 4	11111111 00010010
Operate Line 5	11111111 01010010
Operate Line 6	11111111 00110010
Operate Line 7	11111111 01110010
Operate Line 8	11111111 00001010
Operate Line 9	11111111 01001010
Operate Line 10	11111111 00101010
Operate Line 11	11111111 01101010
Operate Line 12	11111111 00011010
Operate Line 13	11111111 01011010
Operate Line 14	11111111 00111010
Operate Line 15	11111111 01111010
Operate Line 16	11111111 00000110
Operate Line 17	11111111 01000110
Operate Line 18	11111111 00100110
Operate Line 19	11111111 01100110
Operate Line 20	11111111 00010110
Operate Line 21	11111111 01010110
Operate Line 22	11111111 00110110
Operate Line 23	11111111 01110110
Operate Line 24	11111111 00001110
Operate Line 25	11111111 01001110
Operate Line 26	11111111 00101110
Operate Line 27	11111111 01101110
Acknowledge protection switching action	11111111 00011000
Release protection switch	11111111 01100100

Table 2/G.704 – Assigned operations data link messages *(concluded)*

Synchronization:	
G.811	11111111 00100000
G.812 Type II	11111111 00110000
G.812 Type III	11111111 00111110
G.812 Type IV	11111111 00001000
Stratum 4 (Note)	11111111 00010100
G.813 Option 3	11111111 01000100
G.812 Type V	11111111 00011110
Synchronization Traceability Unknown	11111111 00010000
Do not use for Synchronization	11111111 00001100
Provisionable	11111111 00000010
NOTE – Term used in applicable regional standard.	

2.1.3.1.3.1 Priority operations messages

Priority messages are transmitted as continuous repetitions of the designated sequence for the duration of the condition initiating the message. It is permissible to interrupt the continuous repetition of the sequence for an interval not to exceed 100 ms not more then once per second, in order to send one or more other maintenance messages.

Two priority messages have been defined:

- After an LFA condition is detected at local end A, the LFA sequence is transmitted to remote end B for the duration of the LFA condition, but not less than one second.
- A loopback control signal that is used in those applications requiring a continuous enabling signal during operations in a looped condition.

2.1.3.1.3.2 Other maintenance or operations messages

Other maintenance and operations messages are defined in three general categories of loopbacks, protection switching, and synchronization:

- Four types of line loopbacks (in which the entire signal including F-bits is returned to the direction sending the initiation signal) are recognized, three on customer premises and one within the network. Each has a defined sequence to operate. One has a unique sequence to release, while all share a common release sequence. A payload loopback (in which only the information bits in a frame are returned) is defined for implementation in a primary hierarchical level terminal. The F-bits in the return direction are generated by the equipment performing loopback. Unique operate and release sequences are defined. The payload loopback also responds to the universal release sequence.
- For protection switching, 27 sequences are defined to activate protection switching, one sequence is defined to release a protection switch, and one sequence is defined to acknowledge a protection switching action. Activation sequences are of the form $111111110P_1P_2P_3P_4P_510$, where the bit sequence $P_1P_2P_3P_4P_5$ is the binary representation of the decimal line number x of the line to be switched to the protection line. In these sequences, P_1 is the least significant bit of the binary representation.
- Ten messages are reserved for synchronization-related operations. A Synchronization Status Message (SSM) is assigned to each of seven clock types currently or previously defined for 1544 kbits/s systems, and three special-purpose SSM states are defined in addition. In application, a network synchronization distribution system will make use of a subset of the

defined SSMs to reflect the clock types installed in the network and the sync distribution strategy employed.

2.1.3.1.3.3 Performance report from a primary hierarchical level terminal

Performance verification is based on the calculation of CRC checksums and comparison with those received in bits e_1 through e_6 as described in 2.1.3.1.2. These counts, and counts of other events available at the receiving terminal are collected for contiguous one-second periods, summarized and formatted into a performance report message that is returned once each second to the originating terminal in the data link for the opposite direction of transmission.

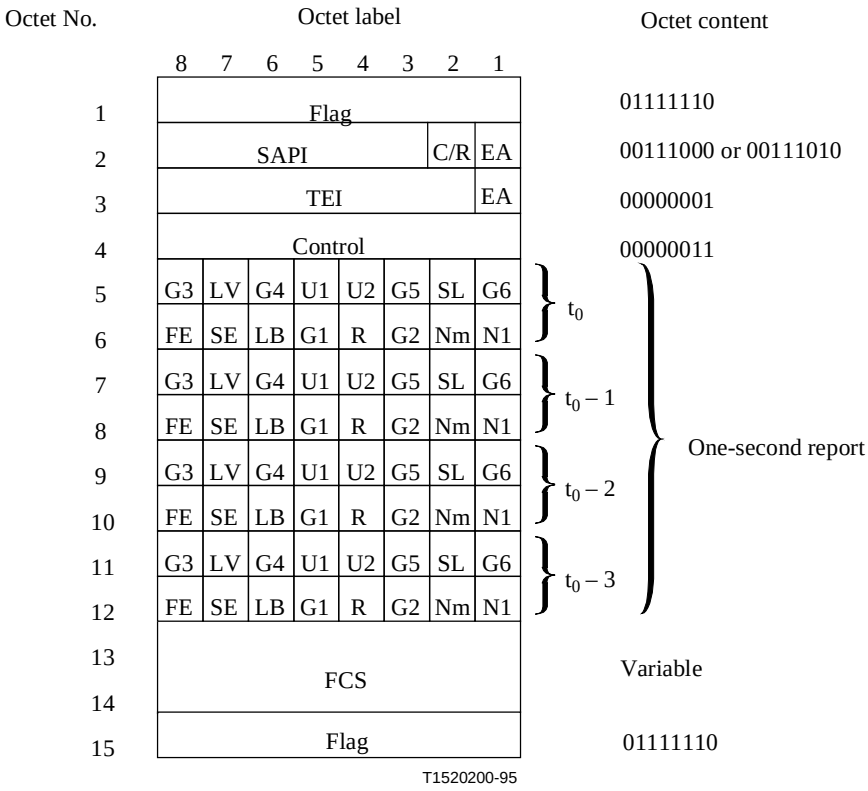
The overall length of the Q.921 frame, including opening and closing flags is 15 bytes. Data on the four most recent seconds is structured into an eight-octet information field as shown in Figure 1. At the end of each one-second accumulation interval, a modulo 4 counter is incremented and the most recent data is examined to set the performance bits in the t_0 octets (octets 5 and 6 of Figure 1). Data from octets 5 and 6 of the previous performance report are moved to octets 7 and 8 of the current report; previous octets 7 and 8 get moved to current octets 9 and 10; previous octets 9 and 10 get moved to current octets 11 and 12, while the previous octets 11 and 12 are discarded.

NOTE 1 – The SAPI value 14 (decimal) is reserved in the 4 kbit/s data link for use in the performance report. The C/R is set to 1 if the terminal originating the report is within the network; the bit is set to 0 if the report originates from within a customer installation. The TEI is set to all zeros. The Extended Address (EA) is always set to 0 in the octet containing the SAPI, and set to 1 in the octet containing the TEI.

The specific values of C/R and TEI defined here are used at the Network Node Interfaces (NNI). Other specific values may be used at local access portion and User-Network Interface (UNI) (see Recommendations G.963 and I.431).

NOTE 2 – The events tracked for the performance report and their definitions are:

- CRC error event – The occurrence of a received set of check bits that differ from the locally generated code.
- Severely-errored framing event – The occurrence of two or more errors in the multiframe alignment sequence within a 3 ms period. Contiguous 3 ms periods shall be examined.
- Frame alignment bit error event – The occurrence of an error in the multiframe alignment signal.
- Line code violation – The occurrence of a bipolar violation.
- Controlled slip event – The occurrence of a controlled frame slip.
- Active payload loopback – The existence of an operative payload loopback in the terminal originating the performance report.



Address	Interpretation
00111000	SAPI = 14, C/R = 0 (CI) EA = 0
00111010	SAPI = 14, C/R = 1 (Carrier) EA = 0
00000001	TEI = 0, EA = 1

Control	Interpretation
00000011	Unacknowledged Information Transfer

One-second report	Interpretation
G1 = 1	CRC Error Event = 1
G2 = 1	1 < CRC Error Event $\leq$ 5
G3 = 1	5 < CRC Error Event $\leq$ 10
G4 = 1	10 < CRC Error Event $\leq$ 100
G5 = 1	100 < CRC Error Event $\leq$ 319
G6 = 1	CRC Error Event $\geq$ 320
SE = 1	Severely-Errored Framing Event $\geq$ 1 (FE shall = 0)
FE = 1	Frame Alignment Bit Error Event $\geq$ 1 (SE shall = 0)
LV = 1	Line Code Violation Event $\geq$ 1
SL = 1	Slip Event $\geq$ 1
LB = 1	Payload Loopback Activated
U1, U2 = 0	Under Study for Synchronization
R = 0	Reserved (Default value is 0)
NmN1 = 00, 01, 10, 11	One-second report modulo 4 counter

FCS	Interpretation
Variable	CRC-16 Frame Check Sequence

NOTE – Rightmost bit transmitted first.

Figure 1/G.704 – Performance report structure at NNI

2.1.3.2 Method 2: 12-frame multiframe

Allocation of the F-bit to the frame alignment signal, multiframe alignment signal and signalling is given in Table 3.

Table 3/G.704 – Allocation of F-bits for the 12-frame multiframe

Frame number	Frame alignment signal	Multiframe alignment signal or signalling
1	1	–
2	–	S
3	0	–
4	–	S
NOTE – For multiframe structure, see 3.1.3.2.2.		

2.2 Basic frame structure at 6312 kbit/s

2.2.1 Frame length

The number of bits per frame is 789. The frame repetition rate is 8000 Hz.

2.2.2 F-bits

The last five bits of a frame are designated as F-bits, and are used for such purposes as frame alignment, performance monitoring and providing a data link.

2.2.3 Allocation of F-bits

Allocation of the F-bits is given in Table 4.

Table 4/G.704 – Allocation of F-bits

Frame number	Bit number				
	785	786	787	788	789
1	1	1	0	0	m
2	1	0	1	0	0
3	x	x	x	a	m
4	e_1	e_2	e_3	e_4	e_5

m Data link bit
a Remote end alarm bit (1 state = alarm, 0 state = no alarm)
e_i CRC-5 check bit (i = 1 to 5)
x Spare bits, to be set at state 1 if not used

2.2.3.1 Frame alignment signal

The frame and multiframe alignment signal is 110010100, and is carried on the F-bits in frames 1 and 2, excluding bit 789 of frame 1.

2.2.3.2 Cyclic redundancy check

The Cyclic Redundancy Check 5 (CRC-5) Message Block (CMB) is a sequence of 3151 serial bits which starts at bit number 1 of frame number 1 and ends at bit number 784 of frame number 4. The CRC-5 message block check bits e_1, e_2, e_3, e_4 and e_5 occupy the last five bits of the multiframe as shown in Table 4.

The check-bit sequence e_1 through e_5 transmitted in multiframe N is the remainder after multiplication by x^5 and then division (modulo 2) by the generator polynomial $x^5 + x^4 + x^2 + 1$ of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_5) is the least significant bit of the remainder. Each multiframe contains the CRC-5 check bits generated for the corresponding CMB.

At the receiver the incoming sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits), when divided by the generator polynomials, will result in a remainder of 00000 in the absence of transmission errors.

2.2.3.3 4 kbit/s data link

The bit m shown in Table 4 is used as a data link bit. These bits provide 4 kbit/s data transmission capability associated with the 6312 kbit/s digital path.

2.2.3.4 Remote end alarm indication

After a loss of frame alignment condition is detected at local end A, remote end alarm signal bit a, shown in Table 4, will be transmitted to remote end B.

2.3 Basic frame structure at 2048 kbit/s

2.3.1 Frame length

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

2.3.2 Allocation of bits number 1 to 8 of the frame

Allocation of bits number 1 to 8 of the frame is shown in Table 5A.

Table 5A/G.704 – Allocation of bits 1 to 8 of the frame

Bit number / Alternate frames	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal	S_i	0	0	1	1	0	1	1
	(Note 1)	Frame alignment signal						
Frame not containing the frame alignment signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	(Note 1)	(Note 2)	(Note 3)	(Note 4)				

NOTE 1 – S_i = Bits reserved for international use. One specific use is described in 2.3.3. Other possible uses may be defined at a later stage. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border. However, they may be used nationally if the digital path does not cross a border.

NOTE 2 – The bit is fixed at 1 to assist in avoiding simulations of the frame alignment signal.

NOTE 3 – A = Remote alarm indication. In undisturbed operation, set to 0; in alarm condition, set to 1.

Table 5A/G.704 – Allocation of bits 1 to 8 of the frame *(concluded)*

NOTE 4 – S_{a4} to S_{a8} = Additional spare bits whose use may be as follows:

i) Bits S_{a4} to S_{a8} may be recommended by ITU-T for use in specific point-to-point applications (e.g. transcoder equipments conforming to Recommendation G.761).

ii) Bit S_{a4} may be used as a message-based data link to be recommended by ITU-T for operations, maintenance and performance monitoring. If the data link is accessed at intermediate points with consequent alterations to the S_{a4} bit, the CRC-4 bits must be updated so as to retain the correct end-to-end path termination functions associated with the CRC-4 procedure (see 2.3.3.5.4). The data-link protocol and messages are for further study.

iii) Bits S_{a5} to S_{a7} are for national usage where there is no demand on them for specific point-to-point applications [see i) above].

iv) One of the bits S_{a4} to S_{a8} may be used in a synchronization interface to convey synchronization status messages, as described in 2.3.4.

Bits S_{a4} to S_{a8} (where these are not used) should be set to 1 on links crossing an international border.

2.3.3 Description of the CRC-4 procedure in bit 1 of the frame

2.3.3.1 Special use of bit 1 of the frame

Where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 should be used for a Cyclic Redundancy Check 4 (CRC-4) procedure as detailed below.

NOTE – Equipment incorporating the CRC-4 procedure should be designed to be capable of interworking with equipment which does not incorporate the CRC-4 procedure, that is, an ability to continue to provide service (traffic) between equipments with and without a CRC-4 capability. This can be achieved either manually (e.g. by straps) or automatically.

– For the manual case, the equipment incorporating the CRC-4 procedure should be capable of fixing bit 1 of the frame to the binary "1" state (see Table 5A, Note 1).

– For the automatic case, this can be achieved at the equipment having the CRC-4 capability either:

  • as a "higher-layer" function under the control of a network management facility (e.g. a TMN) – the details are for further study; or

  • as a "lower-layer" function using a modified CRC-4 multiframe alignment algorithm as described in Annex B/G.706.

2.3.3.2 The allocation of bits 1 to 8 of the frame is shown in Table 5B for a complete CRC-4 multiframe.

Table 5B/G.704 – CRC-4 multiframe structure

	Sub-multiframe (SMF)	Frame number	Bits 1 to 8 of the frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

NOTE 1 – E = CRC-4 error indication bits (see 2.3.3.4)

NOTE 2 – S_{a4} to S_{a8} = Spare bits (see Note 4 to Table 5A)

NOTE 3 – C_1 to C_4 = Cyclic Redundancy Check 4 (CRC-4) bits (see 2.3.3.4 and 2.3.3.5)

NOTE 4 – A = Remote alarm indication (see Table 5A)

2.3.3.3 Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, is divided into two 8-frame Sub-Multiframes (SMF), designated SMF I and SMF II which signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the Cyclic Redundancy Check 4 (CRC-4) block size (i.e. 2048 bits).

The CRC-4 multiframe structure is not related to the possible use of a multiframe structure in 64 kbit/s channel time slot 16 (see 5.1.3.2).

2.3.3.4 Use of bit 1 in 2048 kbit/s CRC-4 multiframe

In those frames containing the frame alignment signal (defined in 2.3.2), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C_1, C_2, C_3 and C_4 in each SMF.

In those frames not containing the frame alignment signal (see 2.3.2), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E).

The CRC-4 multiframe alignment signal has the form 001011.

The E-bits should be set to "0" until both basic frame and CRC-4 multiframe alignment are established (see clause 4/G.706). Thereafter, the E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe.

Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

NOTE 1 – The E-bits will always be taken into account even if the SMF which contains them is found to be errored, since there is little likelihood that the E-bits themselves will be errored.

NOTE 2 – In the short term, there may exist equipments which do not use the E-bits; in this case the E-bits are set to binary 1.

2.3.3.5 Cyclic Redundancy Check (CRC)

2.3.3.5.1 Multiplication/division process

A particular CRC-4 word, located in sub-multiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of sub-multiframe N – 1.

NOTE 1 – When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0, bit 1 or frame 8, bit 1, should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

NOTE 2 – There may be a need to update CRC-4 bits at intermediate equipments which access the S_{a4} bit message-based data-link (see 2.3.3.5.4).

2.3.3.5.2 Encoding procedure

i) The CRC-4 bits in the SMF are replaced by binary 0s.

ii) The SMF is then acted upon by the multiplication/division process referred to in 2.3.3.5.1.

iii) The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

NOTE – The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in i) above, the CRC-4 bit positions in an SMF are initially set to 0 during the multiplication/division process.

2.3.3.5.3 Decoding procedure

i) A received SMF is acted upon by the multiplication/division process referred to in 2.3.3.5.1, after having its CRC-4 bits extracted and replaced by 0s.

ii) The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error free.

2.3.3.5.4 Updating procedure at intermediate path points in a message-based data-link application

The S_{a4} bit may be used as a message-based data-link within 2048 kbit/s paths [see Note 4, ii) to Table 5A]. Situations are envisaged where access to this data link could be required at points on the path between the true path termination points, e.g. reporting of error performance data from intermediate sites along the path. In such situations, it is important that the logical path termination role of CRC-4 is not invalidated or impaired. Hence, any changes to the S_{a4} bits within a SMF at an intermediate path point does not imply a recalculation of the CRC-4 bits over the whole SMF, but rather their update as a linear recoding function in respect of specific deterministic binary changes of the S_{a4} bits only.

Annex C/G.706 gives further information regarding this updating procedure.

2.3.4 Synchronization Status: S_{an}

One of the S_{a4} to S_{a8} bits, (the actual S_a bit is for operator selection), is allocated for Synchronization Status Messages. To prevent ambiguities in pattern recognition, it is necessary to align the first bit (S_{an1}, Table 5C) with frame 1 (Table 5D) of a G.704 multiframe. Table 5C gives the assignment of bit patterns to the four synchronization levels agreed to within ITU-T. Two additional bit patterns are assigned: one to indicate that quality of the synchronization is unknown and the other to indicate that the signal should not be used for synchronization. The remaining codes are reserved for quality levels defined by individual operators.

Table 5D gives the numbering of the S_{an} (n = 4, 5, 6, 7, 8) bits. A S_{an} bit is organized as a 4-bit nibble S_{an1} to S_{an4}. S_{an1} is the most significant bit, S_{an4} is the least significant bit.

NOTE – The message set in S_{an1} to S_{an4} is a copy of the set defined in SDH bits 5 to 8 of byte S1.

Table 5C/G.704 – Synchronization Status Message (SSM) bit allocation for 2048 kbit/s

QL	S_{an1}, S_{an2}, S_{an3}, S_{an4} (Note 1)	Synchronization Quality Level (QL) description
0	0000	Quality unknown (existing synchronization network)
1	0001	Reserved
2	0010	Rec. G.811
3	0011	Reserved
4	0100	SSU-A (Note 2)
5	0101	Reserved
6	0110	Reserved
7	0111	Reserved
8	1000	SSU-B (Note 2)
9	1001	Reserved
10	1010	Reserved
11	1011	Synchronous Equipment Timing Source (SETS)
12	1100	Reserved
13	1101	Reserved
14	1110	Reserved
15	1111	Do not use for synchronization

NOTE 1 – n = 4, 5, 6, 7 or 8 (i.e. one S_a bit only) depending on operator selection.

NOTE 2 – In a previous version of this Recommendation, the terms "G.812 transit" and "G.812 local" were used. These terms were changed to Synchronization Supply Unit (SSU), respectively type A and type B, to align with the clock definitions in Recommendation G.812.

Table 5D/G.704 – S_{an} numbering in Time Slot 0 (TS0) for use in synchronization status message

	Frame number	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
	0	C_1	0	0	1	1	0	1	1
	1	0	1	A	S_{a41}	S_{a51}	S_{a61}	S_{a71}	S_{a81}
S	2	C_2	0	0	1	1	0	1	1
M	3	0	1	A	S_{a42}	S_{a52}	S_{a62}	S_{a72}	S_{a82}
F	4	C_3	0	0	1	1	0	1	1
I	5	1	1	A	S_{a43}	S_{a53}	S_{a63}	S_{a73}	S_{a83}
	6	C_4	0	0	1	1	0	1	1
	7	0	1	A	S_{a44}	S_{a54}	S_{a64}	S_{a74}	S_{a84}
	8	C_1	0	0	1	1	0	1	1
	9	1	1	A	S_{a41}	S_{a51}	S_{a61}	S_{a71}	S_{a81}
S	10	C_2	0	0	1	1	0	1	1
M	11	1	1	A	S_{a42}	S_{a52}	S_{a62}	S_{a72}	S_{a82}
F	12	C_3	0	0	1	1	0	1	1
II	13	E	1	A	S_{a43}	S_{a53}	S_{a63}	S_{a73}	S_{a83}
	14	C_4	0	0	1	1	0	1	1
	15	E	1	A	S_{a44}	S_{a54}	S_{a64}	S_{a74}	S_{a84}

2.4 Basic frame structure at 8448 kbit/s

2.4.1 Frame length

The number of bits per frame is 1056. They are numbered from 1 to 1056. The frame repetition rate is 8000 Hz.

2.4.2 Frame alignment signal

The frame alignment signal is 11100110 100000 and occupies the bit-positions 1 to 8 and 529 to 534.

2.4.3 Service digits

Bit 535 is used to convey alarm indication (bit 535 at 1 state = alarm; bits 535 at 0 state = no alarm).

Bit 536 is left free for national use and should be fixed at 1 on paths crossing the international border. The same applies to bits 9-40 in the case of channel-associated signalling.

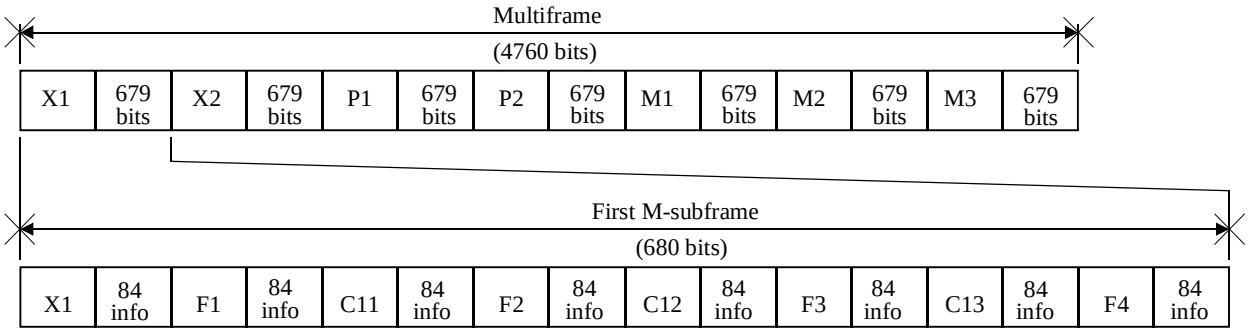
2.5 Basic frame structure at 44 736 kbit/s

2.5.1 Multiframe length

The number of bits per multiframe is 4760 bits.

2.5.2 Multiframe overhead bits

The multiframe are divided into seven M-subframes each with 680 bits; each M-subframe is further divided into 8 blocks of 85 bits: 1 bit for overhead and 84 bits for payload (see Figure 2). Thus, there are 56 overhead bits per multiframe.



The 56 overhead bits sequential positions as follows:							
X1	F1	C11	F2	C12	F3	C13	F4
X2	F1	C21	F2	C22	F3	C23	F4
P1	F1	C31	F2	C32	F3	C33	F4
P2	F1	C41	F2	C42	F3	C43	F4
M1	F1	C51	F2	C52	F3	C53	F4
M2	F1	C61	F2	C62	F3	C63	F4
M3	F1	C71	F2	C72	F3	C73	F4

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Figure 2/G.704 – 44 736 kbit/s multiframe structure

2.5.3 Allocation of the multiframe overhead bits

The overhead bits are the first bit of the eight 85-bit blocks in each of the seven M-subframes in a multiframe, as shown in Figure 2. The 56 overhead bits are: 2 X-bits, 2 P-bits, 3 M-bits, 28 F-bits, and 21 C-bits.

2.5.3.1 X-bits (X1, X2)

X1 and X2 are used to indicate received errored multiframes to the remote end (remote alarm indication "RAI" or "yellow" signal); these bits are set to binary 1 (i.e. X1 = X2 = 1) during error free condition, and to binary 0 (i.e. X1 = X2 = 0) if Loss of Signal (LOS), Out of Frame (OOF), Alarm Indication Signal (AIS), or Slips are detected in the incoming signal. The maximum allowed rate of change of state for the X-bits is once a second; therefore, the X-bits should be set to binary 0 for a length of time equal to the length of the error condition, but rounded-up to the next integer.

2.5.3.2 P-bits (P1, P2)

P1 and P2 are used for performance monitoring; these bits carry parity information calculated over the 4704 payload bits in the preceding multiframe: P1 = P2 = 1 if the digital sum of all payload bits is one, and P1 = P2 = 0 if the digital sum of all payload bits is zero. The P-bits are calculated and may be modified at each section of a facility; therefore, the P-bits provide SECTION performance information, NOT end-to-end performance information.

2.5.3.3 Multiframe alignment signal (M1, M2, M3)

The multiframe alignment signal 010 (M1 = 0, M2 = 1, M3 = 0) is used to locate all seven M-subframes, within the multiframe.

2.5.3.4 M-subframe alignment signal (F1, F2, F3, F4)

The M-subframe alignment signal 1001 (F1 = 1, F2 = 0, F3 = 0, F4 = 1) is used to identify the overhead bit positions.

2.5.3.5 C-bits (C11, C12, C13, C21, ... C_{ij}, ... C73)

In general, 44 736 kbit/s signals could be:

a) unchannelized for bulk data transport; and

b) channelized for multiplex applications.

In either case, the C_{ij} bit positions are available for specific uses, and must be settable by 44 736 kbit/s sources. The way that these C_{ij} bits are used determine the features available in the 44 736 kbit/s signal, through the embedded operations channels:

- The 6312-44 736 kbit/s multiplexing application (M23), uses the C-bits to indicate justification (Recommendation G.752). This Recommendation describes the C-bit Parity application which does not use stuffing bits for justification.
- Both the unchannelized application as well as the channelized C-bit Parity multiplex application[1] use the C-bits as described in 2.5.3.5.1.

2.5.3.5.1 Allocation of C-bits for C-bit Parity application

Regardless of the application (unchannelized or channelized) the C-bits for C-bit Parity application are allocated as follows:

- C11: Application Identification Channel (AIC) – For C-bits Parity application this bit shall be set to binary 1.
- C12: Network Requirements (N_r) – Reserved for future network use. It shall be set to binary 1.
- C13: Far-End Alarm and Control (FEAC) bit is used for two purposes:
  1) Alarm signals to send alarm or status information from the far-end terminal back to the near-end terminal; and
  2) Control signals to initiate 44 736 kbit/s and 1544 kbit/s line loopbacks at the far-end terminal, from the near-end terminal.

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[1] The C-Bit Parity multiplex application for channelized signals uses a two-step multiplexing process to multiplex primary rate signals (1544 or 2048 kbit/s) to the 44 736 kbit/s level. In the first step, four 1544 kbit/s or three 2048 kbit/s lines are multiplexed together to form an integral signal at a bit rate f_e, (pseudo-6312 kbit/s level). In the second step, seven pseudo-6312 kbit/s level, each at a bit rate f_e are multiplexed together to form a 44 736 kbit/s signal with enhanced operations features. The bit rate f_e (nominally 6306.2723) kbit/s) is chosen such that when the seven pseudo-6312 kbit/s level signals are combined, along with "full time" 44 736 kbit/s level justification and the 56-frame overhead bits, the resultant output bit rate will nominally be 44 736 kbit/s. This multiplexing process is the same as that defined for the M23 application except that in the C-bit Parity case all seven intermediate time slots, one in each of the seven M-subframes, are justified at every justification opportunity. Since justification occurs 100% of the time, the C-bits are not needed to denote justification, and they can be used for other purposes.

At international interfaces, initiation of control loopback signal is "optional" and the application of this functionality should be at the discretion of the respective Administrations. The FEAC signal consists of a repeating 16-bit codeword with a general format of 0xxx xxx0 1111 1111, rightmost bit transmitted first (where x can be a 1 or a 0).

To report alarm/status conditions, the 16-bit codeword must be repeated at least 10 times, or while the condition exists, whichever is longer. (Table 6 shows the alarms/status codewords assigned.) These codewords shall be transmitted only after the event has been declared: for example, a 44 736 kbit/s AIS defect would be detected and then timed for several seconds before declaring AIS failure, at which time the appropriate codeword would be transmitted.

To send loopback control commands, two codewords must be sent: the first one – repeated ten times – to activate/de-activate, the other – also repeated ten times – to specify the line number; therefore, each loopback command consists of 20 16-bit codewords. (Table 7 shows the control codewords assigned.) Control words take precedence over alarm signals.

When no alarm/status or control is being transmitted, the FEAC bits must be all set to binary 1.

- C21, C22, C23 – Not used; must be set to binary 1.
- C31, C32, C33 – CP-bits are used to carry path (end-to-end facility) parity information. The Network Terminating Equipment (NTE) that originates the 44 736 kbit/s signal must set these bits (C31 = C32 = C33) to the same value as the P-bits. The CP-bits must not be modified along the 44 736 kbit/s facility path.
- C41, C42, C43 – FEBE-bits are used to carry far-end block error information. All three FEBE bits are set to binary 1 (C41 = C42 = C43 = 1) if no errors are detected in the M-bits, or F-bits, or indicated by the CP-bits. If any error condition (errored M-bits, errored F-bits, or parity in CP-bits) is detected within the multiframe, the FEBE bits must be set to any combination of 1s or 0s (except 111).
- C51, C52, C53 – DL_t bits are used for a 28.2 kbit/s-terminal-to-terminal path maintenance data link. The implementation of this data link is optional but if implemented, it shall conform to the rules set forth in this subclause. The messages carried in the path maintenance data link utilize the frame structure, field definitions, and elements of procedure of the LAPD protocol defined in Recommendation Q.921 but with different addresses. The structure of the LAPD message-oriented signals is defined in Table 8. Table 9 shows the contents and structure of the information field for each of the four message types defined: Common Language Path ID, ITU-T Path ID, Test ID, and Idle Signal ID. The information field contains 6 data elements to identify:

  1) the test type;
  2) the equipment type;
  3) the central office location;
  4) the frame (within the central office);
  5) the unit (within the frame); and
  6) information specific to the test type.

  These signals shall be transmitted continuously at a minimum rate of once per second. When LAPD messages are not being transmitted (i.e. the data link is idle), LAPD flags (01111110) shall be continuously transmitted. If terminal-to-terminal data link function is not implemented, all three bits shall be set to binary 1 (C51 = C52 = C53 = 1). Other applications for the path maintenance data link are for further study.
- C61, C62, C63 – Not used; must be set to binary 1.

- C71, C72, C73 – Not used; must be set to binary 1.

Table 6/G.704 – FEAC alarm/status codewords

FEAC alarm/status codewords	
Alarm/status condition	**Codeword**
Out of frame at 44 736 kbit/s	0000 0000 1111 1111
RDI for HEC-based ATM mapping in 44 736 kbit/s	0000 0010 1111 1111
LCD for HEC-based ATM mapping in 44 736 kbit/s	0000 0100 1111 1111
Equipment failure at 1544 or 2048 kbit/s (NSA)	0000 0110 1111 1111
Equipment failure at 1544 or 2048 kbit/s (SA)	0000 1010 1111 1111
LOS/HBER at 44 736 kbit/s	0001 1100 1111 1111
Equipment failure at 44 736 kbit/s (NSA)	0001 1110 1111 1111
Multiple LOS/HBER at 1544 or 2048 kbit/s	0010 1010 1111 1111
AIS received 44 736 kbit/s	0010 1100 1111 1111
Equipment failure for 44 736 kbit/s (SA)	0011 0010 1111 1111
Idle received at 44 736 kbit/s	0011 0100 1111 1111
Common equipment (NSA)	0011 1010 1111 1111
Single LOS/HBER at 1544 or 2048 kbit/s	0011 1100 1111 1111
NOTE 1 – The rightmost bit of each codeword is transmitted first. NOTE 2 – SA denotes service affecting equipment failure forcing out-of-service state, indicating a defect requiring immediate attention. NOTE 3 – NSA denotes non-service affecting equipment failure indicating a defect in equipment that is not activated, not available, or suspended; it requires attention, but not high priority.	

Table 7/G.704 – FEAC control codeword

FEAC control codewords	
Command	**Codeword**
Activate loopback	0000 1110 1111 1111
De-activate loopback	0011 1000 1111 1111
44 736 kbit/s line	0011 0110 1111 1111
All 1544 or 2048 kbit/s lines	0010 0110 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #1	0100 0010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #1	0100 0100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #1	0100 0110 1111 1111
1544 kbit/s Line No. 4, Group #1	0100 1000 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #2	0100 1010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #2	0100 1100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #2	0100 1110 1111 1111
1544 kbit/s Line No. 4, Group #2	0101 0000 1111 1111

Table 7/G.704 – FEAC control codeword *(concluded)*

FEAC control codewords	
Command	**Codeword**
1544 or 2048 kbit/s Line No. 1, Group #3	0101 0010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #3	0101 0100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #3	0101 0110 1111 1111
1544 kbit/s Line No. 4, Group #3	0101 1000 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #4	0101 1010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #4	0101 1100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #4	0101 1110 1111 1111
1544 kbit/s Line No. 4, Group #4	0110 0000 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #5	0110 0010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #5	0110 0100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #5	0110 0110 1111 1111
1544 kbit/s Line No. 4, Group #5	0110 1000 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #6	0110 1010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #6	0110 1100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #6	0110 1110 1111 1111
1544 kbit/s Line No. 4, Group #6	0111 0000 1111 1111
1544 or 2048 kbit/s Line No. 1, Group #7	0111 0010 1111 1111
1544 or 2048 kbit/s Line No. 2, Group #7	0111 0100 1111 1111
1544 or 2048 kbit/s Line No. 3, Group #7	0111 0110 1111 1111
1544 Line No. 4, Group #7	0111 1000 1111 1111

NOTE 1 – The commands that refer to 1544 or 2048 kbit/s line apply only to a channelized C-bit Parity applications.

NOTE 2 – "Group" refers to the four 1544 kbit/s or three 2048 kbit/s signals that form the intermediate internal f_e signal (see footnote 1); seven of these groups (plus justification) are combined to form the 44 736 kbit/s signal.

NOTE 3 – The rightmost bit of each codeword is transmitted first.

NOTE 4 – To activate or de-activate loopback, the appropriate activate or de-activate 16-bit codeword is transmitted ten times followed immediately by ten repetitions of the 16-bit codeword corresponding to the required line number. Thus, the total length of loopback control message is 20 16-bit words.

Table 8/G.704 – LAPD message structure

Octet no.	Octet label			Octet content
1	Flag			01111110_2
2	SAPI	CR	EA	00111100_2 or 00111110_2
3	TEI		EA	00000001_2
4	Control			00000011_2
	Information field			– Path Identifier (CL or ITU-T), – Idle Signal Id, or – Test Signal Id. – (see Table 9)
N – 1	FCS			See below
N	FCS			

Flag 01111110_2	Interpretation Response Message
SAPI | CR | EA 00111100_2 00111110_2	Interpretation SAPI = 15, C/R = 0 (DTE), EA = 0 SAPI = 15, C/R = 1 (carrier), EA = 0
TEI/EA 00000001_2	Interpretation TEI = 0, EA = 1
Control 00000011_2	Interpretation Fixed value: Unacknowledged Information Transfer
Information field variable	Interpretation See Table 9
FCS Frame Check Sequence	Interpretation CRC-16 Frame Check Sequence, 16-bit code

NOTE – The source of the identification messages shall generate the FCS and the zero stuffing required for transparency. Zero stuffing by a transmitter prevents the occurrence of the flag patten (01111110) in the bits between the opening and closing flags of a frame, by inserting a zero after any sequence of five consecutive ones. The receiver removes a zero following five consecutive ones.

Table 9/G.704 – Information field contents for data-link messages

CL path identification

Data elements	Binary value	
Type	0011 1000 (1 octet)	CL-path ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
CL-facility ID	xxxx xxxx (38 octets)	CL-facility ID

ITU-T path identification

Data elements	Binary value	
Type	0011 1111 (1 octet)	ITU-T path ID
LIC	xxxx xxxx .... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
ITU-T facility ID	xxxx xxxx (44 octets)	ITU-facility ID

Idle signal identification

Data elements	Binary value	
Type	0011 0100 (1 octet)	Idle signal ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
Port no.	xxxx xxxx (38 octets)	Port no.

Test signal identification

Data elements	Binary value	
Type	0011 0010 (1 octet)	Test signal ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
Gen. no.	xxxx xxxx (38 octets)	Generator no.

Location	Uniquely identifies the city and building where the equipment is located.
Frame ID	Uniquely identifies the floor, aisle and bay (within the building) where the equipment is located.
Unit ID	Uniquely identifies the shelf and slot (within the frame) where the card (which generates the signal) is located.
CL-facility ID	Identifies a specific 44 736 kbit/s path, using Common Language conventions and codes.
ITU-T-facility ID	Identifies a specific 44 736 kbit/s path, using Recommendation M.1400 conventions and codes for facility designation.
Port no.	Identifies the equipment port number that initiates the idle signal.
Generator no.	Identifies the equipment generator number that initiates the test signal.

NOTE – The ASCII null character shall be used to indicate the end of the string when the full length of the data field is not needed for a given element. The remaining bit positions of the data element may contain ones, zeros, or any combination of ones and zeros. In those cases where a data element is not needed for a given message, the first octet of the data element shall contain the ASCII null character, the remaining bit positions may contain ones, zeros, or any combination of ones and zeros.

2.5.3.6 Special patterns used at 44 736 kbit/s

Two special patterns are defined for the 44 736 kbit/s signals independently of how the C-bits are used: AIS and IDLE, as described in the following subclauses.

2.5.3.6.1 Alarm Indication Signal (AIS)

The AIS is a signal with valid multiframe and M-subframe alignment signals, and valid P-bits. The information bits are set to a 1010... sequence, starting with a binary one (1) after each M-bit, F-bit, X-bit, P-bit, and C-bit. The C-bits are set to binary zero (C1 = 0, C2 = 0, C3 = 0). The X-bits are set to binary one (X1 = 1, X2 = 1).

2.5.3.6.2 Idle Signal (Idle)

The Idle Signal is a signal with valid multiframe and M-subframe alignment signals, and valid P-bits. The information bits are set to a 1100... sequence, starting with a binary one (1) after each M-bit, F-bit, X-bit, and C-bit. The C-bits are set to binary zero (C1 = 0, C2 = 0, C3 = 0), in the third M-subframe (C31, C32, C33); the remaining C-Bits (three C-bits in M-subframes 1, 2, 4, 5, 6, and 7) may be individually set to one or zero, and may vary with time. The X-bits are set to binary one (X1 = 1, X2 = 1).

3 Characteristics of frame structure carrying channels at various bit rates in 1544 kbit/s

3.1 Interface at 1544 kbit/s carrying 64 kbit/s channels

3.1.1 Frame structure

3.1.1.1 Number of bits per 64 kbit/s channel time slot

Eight, numbered 1 to 8.

3.1.1.2 Number of 64 kbit/s channel time slots per frame

Bits 2 to 193 in the basic frame carry 24 octet interleaved 64 kbit/s channel time slots, numbered 1 to 24.

3.1.1.3 Allocation of F-bit

Refer to 2.1.3.

3.1.2 Use of 64 kbit/s channel time slots

Each 64 kbit/s channel time slot can accommodate, for example, a PCM-encoded voiceband signal conforming to Recommendation G.711 or data information with a bit rate up to 64 kbit/s.

3.1.3 Signalling

Two alternative methods as given in 3.1.3.1 and 3.1.3.2 are recommended.

3.1.3.1 Common channel signalling

One 64 kbit/s channel time slot is used to provide common channel signalling at a rate of 64 kbit/s. In the case of the 12-frame multiframe method of 2.1.3.2, the pattern of the S-bit may be arranged to carry common channel signalling at a rate of 4 kbit/s or a sub-multiple of this rate.

3.1.3.2 Channel associated signalling

3.1.3.2.1 Allocation of signalling bits for the 24-frame multiframe

As can be seen in Table 1, there are four different signalling bits (A, B, C and D) in the multiframe. This channel associated signalling can provide four independent 333-bit/s signalling channels designated A, B, C and D, two independent 667-bit/s signalling channels designated A and B (see Note) or one 1333-bit/s signalling channel.

NOTE – When only four state signalling is required, the A, B signalling bits previously associated with frames 6 and 12 respectively should be mapped into the A, B, C, D signalling bits of frames 6, 12, 18 and 24 respectively as follows: A = A, B = B, C = A, D = B. In this case, the ABCD signalling is the same as the AB signalling specified in 3.1.3.2.2.

3.1.3.2.2 Allocation of signalling bits for the 12-frame multiframe

Based on agreement between the Administrations involved, channel-associated signalling is provided for intra-regional circuits according to the following arrangement.

A multiframe comprises 12 frames as shown in Table 10. The multiframe alignment signal is carried on the S-bit as shown in the table.

Frames 6 and 12 are designated as signalling frames. Bit eight in each channel time slot is used in every signalling frame to carry the signalling associated with that channel.

Table 10/G.704 – Multiframe structure

Frame number	Frame alignment signal (Note 1)	Multiframe alignment signal (S-bit)	Bit number(s) in each channel time slot		Signalling channel designation (Note 2)
			For character signal	For signalling	
1	1	–	1-8	–	
2	–	0	1-8	–	
3	0	–	1-8	–	
4	–	0	1-8	–	
5	1	–	1-8	–	
6	–	1	1-7	8	A
7	0	–	1-8	–	
8	–	1	1-8	–	
9	1	–	1-8	–	
10	–	1	1-8	–	
11	0	–	1-8	–	
12	–	0	1-7	8	B

NOTE 1 – When the S-bit is modified to signal the alarm indications to the remote end, the S-bit in frame 12 is changed from state 0 to 1.

NOTE 2 – Channel-associated signalling provides two independent 667-bit/s signalling channels designated A and B or one 1333-bit/s signalling channel.

3.2 Interface at 1544 kbit/s carrying 32 kbit/s channel time slots (see Note)

NOTE – This interface provides for the carrying of 32 kbit/s information. The interface will be used between network nodes and will apply to primary rate multiplexing equipment, digital cross-connect equipment, transcoder and other equipment relevant to the network nodes. Switching in this case is assumed to take place on a 64 kbit/s basis.

3.2.1 Frame structure

3.2.1.1 Number of bits per 32 kbit/s channel time slot

Four, numbered 1 to 4.

3.2.1.2 Number of 32 kbit/s channel time slots per frame

Bits 2 to 193 in the basic frame can carry forty-eight 4-bit interleaved 32 kbit/s channel time slots, numbered 1 to 48.

3.2.1.3 Allocation of F-bits

Refer to 2.1.3.

3.2.2 Use of 32 kbit/s channel time slot

Each 32 kbit/s channel time slot can accommodate an ADPCM-encoded voiceband signal conforming to Recommendation G.721, or data with a bit rate up to 32 kbit/s.

3.2.3 384 kbit/s 12-channel time slot grouping

3.2.3.1 Structure of 12-channel time slot grouping

The 1544 kbit/s frame for 32 kbit/s channel time slots shown in Table 11 is structured to provide four independent 384 kbit/s 12-channel time slot groupings. These are numbered 1-4, and transmitted in numbered order starting with time slot grouping number 1.

The Signalling Grouping Channels (SGC) for time slot groupings 1-4, occupy time slots 12, 24, 36 and 48, respectively. Each time slot grouping can be independently configured for situations requiring channel-associated signalling or situations with no signalling requirement (e.g. external common signalling). (See 3.2.3.1.1.)

Table 11/G.704 – 32 kbit/s channel time slots frame structure for 1544 kbit/s interface

Time slot grouping	Time slots												
No. 1	1	2	3	4	5	6	7	8	9	10	11	12	(SGC)
No. 2	13	14	15	16	17	18	19	20	21	22	23	24	(SGC)
No. 3	25	26	27	28	29	30	31	32	33	34	35	36	(SGC)
No. 4	37	38	39	40	41	42	43	44	45	46	47	48	(SGC)

NOTE 1 – Each time slots signifies a 32 kbit/s channel.

NOTE 2 – The Signalling Grouping Channel (SGC) occupies the twelfth 32 kbit/s time slot of each time slot grouping.

3.2.3.1.1 Use of a 384 kbit/s time slot grouping

Use of a 384 kbit/s time slot grouping is categorized into two possible configurations:

– When no signalling capabilities are required, a 384 kbit/s time slot grouping can carry twelve 32 kbit/s channel time slots.

– When channel-associated signalling capabilities are required, a 384 kbit/s time slot grouping will consist of eleven 32 kbit/s channel time slots and a 32 kbit/s channel time slot defined as a signalling grouping channel.

3.2.3.1.2 Use of a signalling grouping channel

A signalling grouping channel is used for the transmission of channel-associated A-B-C-D signalling information, signalling grouping channel alarm information, the signalling grouping channel multiframe alignment signal, and CRC-6 error detection information between network nodes.

3.2.4 32 kbit/s signalling grouping channel multiframe structure

3.2.4.1 Number of bits per 32 kbit/s signalling grouping channel time slot

Four, numbered 1 to 4.

3.2.4.2 Bit allocation of 32 kbit/s signalling grouping channel time slot

Allocated to the last four bits of each time slot grouping.

3.2.4.3 Multiframe structure

The signalling grouping channel multiframe structure consists of 24 consecutive frames numbered 1 to 24. Table 12 shows the signalling grouping channel multiframe structure.

Table 12/G.704 – 32 kbit/s signalling grouping channel multiframe structure

Time slot grouping frame number	Signalling grouping channel bit number			
	1	**2**	**3**	**4**
1	A_j	A_{j+1}	0	S_1
2	A_{j+2}	A_{j+3}	1	S_2
3	A_{j+4}	A_{j+5}	0	CRC-1
4	A_{j+6}	A_{j+7}	1	S_4
5	A_{j+8}	A_{j+9}	0	S_5
6	A_{j+10}	M_1	1	S_6
7	B_j	B_{j+1}	0	CRC-2
8	B_{j+2}	B_{j+3}	1	S_8
9	B_{j+4}	B_{1+5}	0	S_9
10	B_{j+6}	B_{j+7}	1	S_{10}
11	B_{j+8}	B_{j+9}	0	CRC-3
12	B_{j+10}	M_2	1	S_{12}

Table 12/G.704 – 32 kbit/s signalling grouping channel multiframe structure *(concluded)*

Time slot grouping frame number	Signalling grouping channel bit number			
	1	**2**	**3**	**4**
13	C_j	C_{j+1}	1	S_{13}
14	C_{j+2}	C_{j+3}	0	S_{14}
15	C_{j+4}	C_{1+5}	1	CRC-4
16	C_{j+6}	C_{j+7}	0	S_{16}
17	C_{j+8}	C_{j+9}	1	S_{17}
18	C_{j+10}	M_2	0	S_{18}
19	D_j	D_{j+1}	1	CRC-5
20	D_{j+2}	D_{j+3}	0	S_{20}
21	D_{j+4}	D_{1+5}	1	S_{21}
22	D_{j+6}	D_{j+7}	0	S_{22}
23	D_{j+8}	D_{j+9}	1	CRC-6
24	D_{j+10}	M_4	0	S_{24}

NOTE 1 – j = 1 for 12th 32 kbit/s channel time slot.
j = 13 for 24th 32 kbit/s channel time slot.
j = 25 for 36th 32 kbit/s channel time slot.
j = 37 for 48th 32 kbit/s channel time slot.

NOTE 2 – (A_j, B_j, C_j, D_j) A, B, C, D signalling bits.
M_j Signalling grouping channel alarm indication bits.
S_k Spare bits.

NOTE 3 – The signalling grouping channel provides A, B, C, D signalling capability for 11 channels within each time slot grouping.

3.2.4.4 Signalling grouping channel multiframe alignment signal

Bit 3 of the signalling grouping channel, as shown in Table 12, contains the signal grouping channel multiframe alignment signal used to associate the signalling bits in the signal grouping channel with the proper channels of the associated time slot grouping.

NOTE – The signalling grouping channel multiframe alignment signal is independent of, and different from the framing bit of the 1544 kbit/s frame.

3.2.4.5 CRC-6 error detection information for the time slot grouping

An optional 2 kbit/s CRC-6 error detection codeword may be transmitted in the bit-position indicated by CRC-1 through CRC-6 in Table 12.

The CRC-6 Message Block (CMB) is a sequence of 1152 serial bits that is coincident with a time slot grouping multiframe. By definition, CMB N begins at bit-position 0 of time slot grouping multiframe N and ends at bit-position 1151 of time slot grouping multiframe N.

The check-bit sequence CRC-1 through CRC-6 transmitted in multiframe N + 1 is the remainder after multiplication by x^6, and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the polynomial corresponding to CMB N. The first check bit, CRC-1, is the most significant bit of the remainder; the last check bit CRC-6, is the least significant bit. The time slot grouping channel is included in this calculation with bit 4 of the time slot grouping channel being set to 1.

When not utilizing the option to transmit the CRC-6 error detection signal, CRC-1 through CRC-6 shall be set to 1.

3.2.4.6 Signalling

Two alternative methods as given in 3.2.4.6.1 and 3.2.4.6.2 are recommended.

3.2.4.6.1 Common channel signalling

Refer to 3.1.3.1. Two successive 32 kbit/s channel time slots are used for 64 kbit/s common channel signalling transmission.

3.2.4.6.2 Channel associated signalling

As indicated in Table 12, bits 1 and 2 of the signalling grouping channel convey the channel-associated signalling information for the channels of the associated time slot grouping.

The signalling grouping channel can provide four independent 333 bit/s signalling channels designated A, B, C and D, two independent 667 bit/s signalling channels designated A and B, or one 1333 bit/s signalling channel designated A. Where only A-B signalling is used, the A-B signalling is repeated for the C-D positions respectively. Where only A signalling is used, the A signalling is repeated for the B-C-D positions respectively.

3.2.4.7 Signalling grouping channel alarm indication signals

As indicated in Table 12, the signalling grouping channel contains four alarm indication bits, M_1, M_2, M_3 and M_4.

M_1 provides the capability to transmit through the interface a remote time slot grouping alarm indication of a failure in the opposite direction of transmission.

M_2 provides the capability to transmit through the interface an indication of a failure in tributary input signals to the network node.

M_3 provides the capability to transmit through the interface an indication of a failure in tributary output signals from the network node.

M_4 is set to 1 whenever M_1 and/or M_2 and/or M_3 are set to 1.

3.2.5 Signal grouping channel unused bits

The bits marked S in Table 12 are currently unused and set to 1. The definition and allocation of the S-bits are for further study.

3.2.6 Loss and recovery of signalling channel multiframe alignment

Loss of the signalling grouping channel multiframe alignment signal is declared when two out of four signalling grouping channel framing bits are in error. The rare occurrence of a single instantaneous slip of ± 11 frames is undetected by the two-out-of-four algorithm. Signalling grouping channel multiframe alignment shall be declared when the correct sequence of 24 valid signalling grouping channel framing bits is detected, beginning with the first frame of the multiframe.

3.3 Interface at 1544 kbit/s carrying n × 64 kbit/s

Electrical characteristics should follow Recommendation G.703.

The time slot mapping to the 1544 kbit/s interface is for further study.

4 Characteristics of frame structures carrying channels at various bit rates in 6312 kbit/s interfaces

4.1 Interface at 6312 kbit/s carrying 64 kbit/s channels

4.1.1 Frame structure

4.1.1.1 Number of bits per 64 kbit/s channel time slot

Eight, numbered 1 to 8.

4.1.1.2 Number of 64 kbit/s channel time slots per frame

Bits 1 to 784 in the basic frame carry 98 octet interleaved 64 kbit/s channel time slots, numbered 1 to 98. Five bits per frame (F-bits) are added at the end of the frame for the frame alignment signal and for other signals.

4.1.1.3 Allocation of the F-bits

Refer to Table 4.

4.1.2 Use of 64 kbit/s channel time slots

Each 64 kbit/s channel time slot can accommodate, for example, a PCM-encoded voiceband signal conforming to Recommendation G.711 or data information with a bit rate up to 64 kbit/s. 64 kbit/s channel time slots 97, 98 may be used for signalling.

4.1.3 Signalling

Two alternative methods as given in 4.1.3.1 and 4.1.3.2 are recommended.

4.1.3.1 Common channel signalling

Use of 64 kbit/s channel time slots 97 and 98 for common channel signalling is under study.

4.1.3.2 Channel-associated signalling

Based on agreement between the Administrations concerned, channel-associated signalling is provided for intra-regional circuits according to the following arrangement.

4.1.3.2.1 Allocation of signalling bit

Sixteen signalling bits (bit-positions 769 to 784) are designated as ST_1 to ST_{16}. One ST_i-bit (i = 1 to 16) accommodates signalling information corresponding to six channel time slots i, 16 + i, 32 + i, 48 + i, 64 + i and 80 + i in a manner described in 4.1.3.2.2 below.

4.1.3.2.2 Signalling multiframe structure

Each ST-bit constitutes an independent signalling multiframe over eight frames as shown in Table 13.

Table 13/G.704 –Signalling multiframe structure

Frame number	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
Use of ST-bit	F_s	S_1	S_2	S_3	S_4	S_5	S_6	S_p
	(Note 1)	(Note 2)						(Note 4)

NOTE 1 – The F_s-bit is either alternate 0, 1 or the following 48 bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48-bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$x^7 + x^4 + 1$$

NOTE 2 – S_j-bit (j = 1 to 6) carry channel-associated signalling or maintenance information. When the 48-bit pattern is adopted as the F_s frame alignment signal, each S_j-bit (j = 1 to 6) can be multiframed, as follows:

$$S_{j1}, S_{j2}, ..., S_{j12}$$

The S_{j1}-bit carries the following 16-bit frame alignment pattern generated according to the same primitive polynomial as for the 48-bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each S_{ji}-bit (i = 2 to 12) carries channel-associated signalling for sub-rate circuits and/or maintenance information.

NOTE 3 – ST-bits (F_s, S_1, ..., S_6 and S_p), all at state 1 indicate Alarm Indication Signal (AIS) for six 64 kbit/s channels.

NOTE 4 – The S_p-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required to be sent, the S_p is set to state 0.

4.2 Interfaces at 6312 kbit/s carrying other channels than 64 kbit/s

For further study.

5 Characteristics of frame structures carrying channels at various bit rates in 2048 kbit/s interfaces

5.1 Interface at 2048 kbit/s carrying 64 kbit/s channels

5.1.1 Frame structure

5.1.1.1 Number of bits per 64 kbit/s channel time slot

Eight, numbered 1 to 8.

5.1.1.2 Number of 64 kbit/s channel time slots per frame

Bits 1 to 256 in the basic frame carry 32-octet interleaved time slots numbered 0 to 31.

5.1.1.3 Allocation of the bits of 64 kbit/s channel time slot 0

See Table 5A in 2.3.2.

5.1.2 Use of other 64 kbit/s channel time slots

Each of the 64 kbit/s channel time slots 1 to 15 and 17 to 31 can accommodate, for example, a PCM-encoded voiceband signal according to Recommendation G.711 or a 64 kbit/s digital signal.

The 64 kbit/s channel time slot 16 may be used for signalling. If not needed for signalling, in some cases it may be used for a 64 kbit/s channel in the same way as time slots 1 to 15 and 17 to 31.

5.1.3 Signalling

The use of 64 kbit/s channel time slot 16 is recommended for either common channel or channel-associated signalling as required.

The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

5.1.3.1 Common channel signalling

The 64 kbit/s channel time slot 16 may be used for common channel signalling systems up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

5.1.3.2 Channel-associated signalling

This subclause contains the recommended arrangement for the use of the 64 kbit/s capability of channel time slot 16 for channel-associated signalling.

5.1.3.2.1 Multiframe structure

A multiframe comprises 16 consecutive frames (whose structure is given in 5.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

5.1.3.2.2 Allocation of 64 kbit/s channel time slot 16

When 64 kbit/s channel time slot 16 is used for channel-associated signalling, the 64 kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignment signal as a reference.

Details of the bit allocation are given in Table 14.

Table 14/G.704 – Bit allocation of channel associated 64 kbit/s time slot 16 for channel-associated signalling

Time slot 16 of frame 0	Time slot 16 of frame 1		Time slot 16 of frame 2		– – –	Time slot 16 of frame 15	
0000xyxx	abcd channel 1	abcd channel 16	abcd channel 2	abcd channel 17	– – –	abcd channel 15	abcd channel 30

NOTE 1 – Channel numbers refer to telephone channel numbers. 64 kbit/s channel time slots 1 to 15 and 17 to 31 are assigned to telephone channels numbered from 1 to 30.

NOTE 2 – This bit allocation provides four 500 bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

NOTE 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended that the combination 0000 of bits a, b, c and d should not be used for signalling purposes for channels 1 to 15.

NOTE 4 – x = Spare bit, to be set to 1 if not used.

y = Bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

5.2 Interface at 2048 kbit/s carrying n × 64 kbit/s

Electrical characteristics should follow Recommendation G.703 (see clause 6/G.703). For the accommodation of n × 64 kbit/s time slots in the 2048 kbit/s frame, two situations are envisaged.

5.2.1 One n × 64 kbit/s signal on the tributary side of a multiplex equipment

Time slots of the 2048 kbit/s frame are filled as follows:

- TS0: According to 2.3;
- TS16: Reserved for the accommodation, if required, of a 64 kbit/s signalling channel.
  - If 2 < n < 15, TS1 to TSn are filled with n × 64 kbit/s data [see Figure 3 a)];
  - If 15 < n < 30, TS1 to TS15 and TS17 to TS(n + 1) are filled with n × 64 kbit/s data [see Figure 3 b)].
  - Remaining time slots are filled with all 1s.

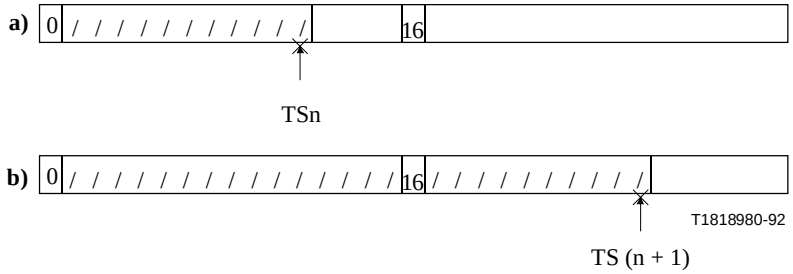

Figure 3/G.704

5.2.2 One or more n × 64 kbit/s signal on the multiplexed signal side of a multiplexing equipment

For any one n × 64 kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

- TS0: According to 2.3;
- TS16: Reserved for the accommodation, if required, of a 64 kbit/s signalling channel.

TS (x) of the 2048 kbit/s frame is designated as the time slot into which the first time slot of the n × 64 kbit/s is accommodated.

– If $x < 15$ and $x + (n - 1) < 15$, or, if $x^3 > 17$ and $x + (n - 1) < 31$, then the filling of time slots is from TS (x) to TS (x + n – 1) [see Figure 4 a) and b)];

– If $x + (n - 1)^3 > 16$, then the filling of time slots is from TS (x) to TS15 and TS17 to TS (x + n) [see Figure 4 c)].

NOTE – Once n × 64 kbit/s signal has been accommodated into the multiplexed signal, care should be taken in the interpretation of the above rules to ensure that further such signals only use the time slots which remain spare.

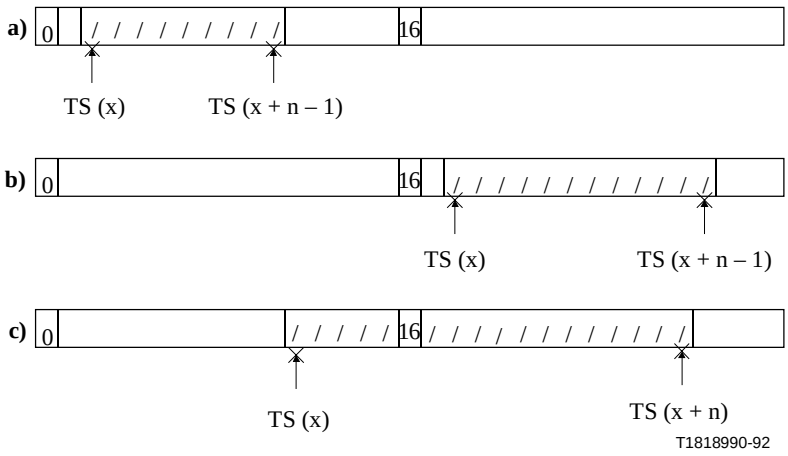

Figure 4/G.704

6 Characteristics of frame structures carrying channels at various bit rates in 8448 kbit/s interface

6.1 Interface at 8448 kbit/s carrying 64 kbit/s channels

6.1.1 Frame structure

6.1.1.1 Number of bits per 64 kbit/s channel time slot

Eight, numbered from 1 to 8.

6.1.1.2 Number of 64 kbit/s channel time time slots per frame

Bits 1 to 1056 in the basic frame carry 132 octet interleaved 64 kbit/s channel time slots, numbered from 0 to 131.

6.1.2 Use of 64 kbit/s channel time slots

6.1.2.1 64 kbit/s channel time slot assignment in case of channel-associated signalling

64 kbit/s channel time slots 5 to 32, 34 to 65, 71 to 98 and 100 to 131 are assigned to 120 telephone channels from 1 to 120.

64 kbit/s channel time slot 0 and the first 6 bits in 64 kbit/s channel time slot 66 are assigned to framing: the remaining 2 bits in 64 kbit/s channel time slot 66 are devoted to services.

64 kbit/s channel time slots 67 to 70 are assigned to channel-associated signalling as covered in 6.1.4.2 below.

64 kbit/s channel time slots 1 to 4, 33 are left free for national use.

6.1.2.2 64 kbit/s channel time slot assignment in case of common channel signalling

64 kbit/s channel time slots 2 to 32, 34 to 65, 67 to 98 and 100 to 131 are available for 127 telephone, signalling or other service channels. By bilateral agreement between the Administrations concerned, 64 kbit/s channel time slot 1 may either be used to provide another telephone or service channel or left free for service purposes within a digital exchange.

The 64 kbit/s channels corresponding to 64 kbit/s channel time slot 1 to 32, 34 to 65 (etc., as above) are numbered 0 to 127.

64 kbit/s channel time slot 0 and the first 6 bits in channel time slot 66 are assigned to framing, the remaining 2 bits in 64 kbit/s channel time slot 66 are assigned to service.

64 kbit/s channel time slots 67 to 70 are, in descending order of priority, available for common channel signalling as covered in 6.1.4.1 below.

64 kbit/s channel slot 33 is left free for national use.

6.1.3 Description of the CRC procedure in 64 kbit/s channel time slot 99

In order to provide an end-to-end quality monitoring of the 8 Mbit/s link, a CRC-6 procedure is used and the six bits C_1 to C_6 computed at the source location are inserted in bit-positions 1 to 6 of the time slot 99 (see Figure 5).

In addition, bit 7 of this time slot, denoted E, is used to send in the transmitting direction an indication about the received signal arriving from the opposite direction. Bit-E indicates whether or not the most recent CRC block arriving at the opposite end had errors.

The CRC-6 bits C_1 to C_6 are computed for each frame. The CRC-6 block size is then 132 octets, i.e. 1056 bits, and the computation is made 8000 times per second.

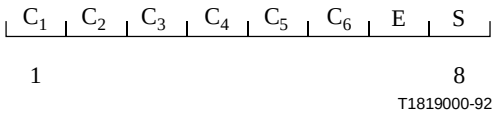

Figure 5/G.704 – Time slot 99

6.1.3.1 Multiplication/division process

A given C_1-C_6 word located in frame N is the remainder after multiplication by x^6 and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the polynomial representation of frame (N – 1).

NOTE – When representing the contents of a frame as a polynomial, the first bit in the frame should be taken as being the most significant bit. Similarly C_1 is defined to be the most significant bit of the remainder and C_6 the least significant bit of the remainder.

6.1.3.2 Encoding procedure

The CRC bit positions are initially set at 0, i.e.:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0$$

The frame is then acted upon by the multiplication/division process referred to above in 6.1.3.1.

The remainder resulting from the multiplication/division process is stored ready for insertion into the respective CRC locations of the next frame.

NOTE – These CRC bits do not affect the computation of the CRC bits in the next frame since the corresponding locations are set to 0 before the computation.

6.1.3.3 Decoding procedure

A received frame is acted upon by the multiplication/division process, referred to above in 6.1.3.1, after having its CRC bits extracted and replaced by 0s.

The remainder resulting from this multiplication/division process is then stored and subsequently compared on a bit-by-bit basis with the CRC received in the next frame.

If the decoder-calculated remainder exactly corresponds to the CRC bits sent from the encoder, it is assumed that the checked frame is error free.

6.1.3.4 Action on bit-E

Bit-E of frame N is set to 1 in the transmitting direction if bits C_1 to C_6, detected in the most recent frame at the opposite end, have been found in error (at least one bit in error). If no errors, E is set to 0.

6.1.4 Signalling

The use of channel time slots 67 to 70 is recommended for either common channel or channel-associated signalling as required. The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

6.1.4.1 Common channel signalling

64 kbit/s channel time slots 67 to 70 may be used for common channel signalling in a descending order of priority up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

6.1.4.2 Channel-associated signalling

The recommended arrangement for the use of the 64 kbit/s capacity in each 64 kbit/s channel time slot 67 to 70 for channel-associated signalling is as follows.

6.1.4.2.1 Multiframe structure

A multiframe for each 64 kbit/s bit-stream comprises 16 consecutive frames (whose structure is given in 6.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of channel time slots 67 to 70 in frame 0.

6.1.4.2.2 Allocation of 64 kbit/s channel time slots 67 to 70

When 64 kbit/s channel time slots 67 to 70 are used for channel-associated signalling, the 64 kbit/s capacity of each of the four 64 kbit/s channel time slots is sub-multiplexed into lower-rate signalling channels using the multiframe alignment signal as a reference. Details of the bit allocation are given in Table 15.

Table 15/G.704 – Bit allocation of 64 kbit/s channel time slots 67 to 70

64 kbit/s channel time slots **Frame**	**67**		**68**		**69**		**70**	
0	0000xyxx		0000xyxx		0000xyxx		0000xyxx	
1	abcd channel 1	abcd channel 16	abcd channel 31	abcd channel 46	abcd channel 61	abcd channel 76	abcd channel 91	abcd channel 106
	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
15	abcd channel 15	abcd channel 30	abcd channel 45	abcd channel 60	abcd channel 75	abcd channel 90	abcd channel 105	abcd channel 120

NOTE 1 – Channel numbers refer to telephone channel numbers. Refer to 6.1.2.1 for the assignment of 64 kbit/s channel time slots to the telephone channels.

NOTE 2 – This bit allocation provides four 500 bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

NOTE 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended that the combination 0000 of bits a, b, c and d should not be used for signalling purposes for channels 1-15, 31-45, 61-75 and 91-125.

NOTE 4 – x = Spare bit, to be set to 1 if not used.

y = Bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

6.2 Interface at 8448 kbit/s carrying other channels than 64 kbit/s

For further study.

ANNEX A

Examples of CRC implementations using shift registers

A.1 CRC-6 procedure for interface at 1544 kbit/s (see 2.1.3.1.2)

See Figure A.1.

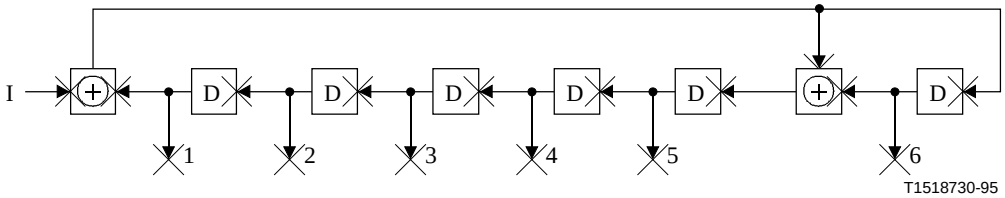

Figure A.1/G.704

Input I to the shift register: CMB N with F-bits set to 1.

Generator polynomial of the shift register: $x^6 + x + 1$.

At I, the CMB is fed serially (i.e. bit-by-bit) into the circuit, starting with bit number 1 of the multiframe (see Table 1). When the last bit of the CMB (i.e. bit number 4632 within the multiframe) has been fed into the shift register, the CRC bits e_1 to e_6 are available at the outputs 1 to 6. (Output 1 provides the most significant bit, e_1, and output 6 the least significant bit, e_6.) Bits e_1 to e_6 are transmitted in the next CMB (see Table 1).

NOTE – The outputs (1 to 6) of the shift register stages are reset to 0 after each CMB.

A.2 CRC-5 procedure for interface at 6312 kbit/s (see 2.2.3.2)

See Figure A.2.

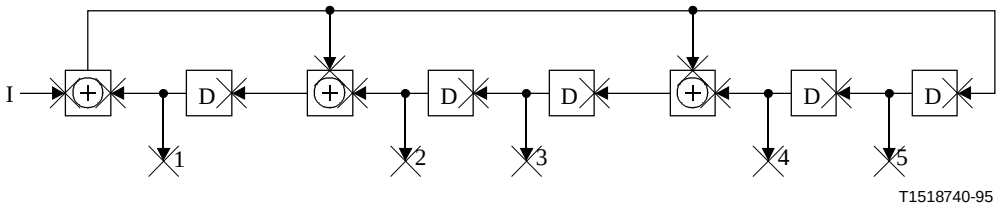

Figure A.2/G.704

Input I to the shift register: CMB N.

Generator polynomial of the shift register: $x^5 + x^4 + x^2 + 1$.

At I, the CMB is fed serially (i.e. bit-by-bit) into the circuit, starting with bit number 1 of frame number 1 (see Table 4). When the last bit of the CMB (i.e. bit number 784 of frame number 4) has been fed into the shift register, the CRC bits e_1 to e_5 are available at the outputs 1 to 5. (Output 1 provides the most significant bit, e_1, and output 5 the least significant bit, e_5.) Bits e_1 to e_5 are transmitted in the corresponding multiframe (see Table 4).

NOTE – The outputs (1 to 5) of the shift register stages are reset to 0 after each CMB.

A.3 CRC-4 procedure for interface at 2048 kbit/s (see 2.3.3.5)

See Figure A.3.

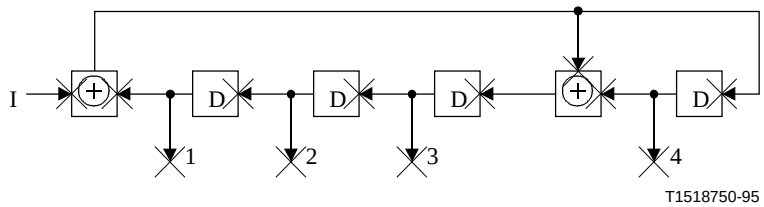

Figure A.3/G.704

Input I to the shift register: SMF(N) with C_1, C_2, C_3, C_4 set to 0.

Generator polynomial of the shift register: $x^4 + x + 1$.

At I, the SMF is fed serially (i.e. bit-by-bit) into the circuit, starting with bit $C_1 = 0$ (see Table 5B). When the last bit of the SMF (i.e. bit number 256 of frame number 7, or frame number 15) has been fed into the shift register, the CRC bits C_1 to C_4 are available at the outputs 1 to 4. (Output 1 provides the most significant bit, C_1, and output 4 the least significant bit, C_4.) Bits C_1 to C_4 are transmitted in the next SMF, i.e. SMF(N + 1).

NOTE – The outputs (1 to 4) of the shift register stages are reset to 0 after each SMF.

ANNEX B

Alphabetical list of abbreviations used in this Recommendation

AIS Alarm Indication Signal

CRC Cyclic Redundancy Check

DL Data Link

FAS Frame Alignment Signal

LFA Loss of Frame Alignment

SGC Signalling Grouping Channel

SMF Sub-Multiframe

SSU Synchronization Supply Unit

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