PDH vs. SDH

(PDH = Plesiochronous Digital Hierarchy)
(SDH = Synchronous Digital Hierarchy)

• Why is SDH replacing PDH systems?
• (1) greater flexibility in cross-connecting and demultiplexing of tributaries
• (2) more advanced network management is possible using SDH, partly due to (1)
Case study:

140 Mbit/s PDH

155 Mbit/s STM-1

from

get

2 Mbit/s signal

155 Mbit/s STM-1

2 Mbit/s signal

140 Mbit/s PDH

2 Mbit/s signal

2 Mbit/s signal
PDH multiplexing

Example: four independent and mutually unsynchronized 2.048 Mbit/s signals (tributaries) are multiplexed into a single 8.448 Mbit/s signal using positive/zero/negative justification (bit stuffing) according to ITU-T Rec. G.745.

Further multiplexing is accomplished in a similar way:
- four 8.448 Mbit/s signals into a 34.368 Mbit/s signal
- four 34.368 Mbit/s signals into a 139.264 Mbit/s signal.

Consequently, a 140 Mbit/s signal can consist of a total of 64 independent 2 Mbit/s signals.
PDH multiplexing cont.

When 64 independent and unsynchronized 2.048 Mbit/s tributaries are multiplexed into one 139.264 Mbit/s signal, a total of $4 + 16 + 64 = 84$ “multiplex circuits” are needed.

When a 139.264 Mbit/s signal is demultiplexed into 2.048 Mbit/s signals, a total of 84 clock synchronization circuits and “demultiplex circuits” are needed.

When a single 2.048 Mbit/s signal is demultiplexed from a 139.264 Mbit/s signal, three clock synchronization and demultiplex circuits are needed.
8.448 Mbit/s multiplex frame structure

- Cyclic bit interleaving
- Frame length 1056 bits
- FAS
- Justification control bits
- Justification bits
4 : 1 multiplex circuit

- CL in: 2 Mb/s
- Elastic buffer
- Inhibit clock cycle (empty justification bit)
- CL out: 8 Mb/s
- 4 : 1 MUX
- other 2 Mb/s tributaries
- Fixed overhead (FAS…)

inhibit clock cycle in CL out in specific bit interval when elastic buffer is running out of contents
1:4 demultiplex circuit

8 Mb/s
1:4 DEMUX

other 2 Mb/s tributaries

CL in
Elastic buffer
Inhibit clock cycle if empty justification bit

2 Mb/s
PLL

CL out
SDH multiplexing (ITU-T G.707)

- We are again concerned with only one 2.048 Mbit/s signal (30 channel PCM system)
- The remaining 2.048 Mbit/s signals may be independent and mutually unsynchronized, as in the PDH case.

2.048 Mbit/s signal to VC-12 (mapping)
VC-12 to TU-12 (pointer processing)
TU-12 to TUG-2 to TUG-3 to VC-4 (multiplexing)
VC-4 to AU-4 (pointer processing)
AU-4 to STM-1 (multiplexing)
NOTE - G.702 tributaries associated with containers C-x are shown. Other signals, e.g. ATM, can also be accommodated (see 10.2).

Organizing PDH signals into an STM-1 frame (N = 1)
Basic STM-1 frame structure \((N = 1)\)
Basic STM-1 frame structure (N = 1)
Organization of STM-1 frame

- **SOH**: Start of Frame Head
- **STM-1 payload**: Contains data
- **pointer**: Indicates location of VC-12
- **VC-4**: Virtual Container
  - **POH** (Path Overhead)
  - **Virtual container (VC)**
- **TU-12**: Virtual tributary unit
- **VC-12**: Virtual tributary container

Fixed location distributed in four columns within the VC-4.
SDH terminology

**SOH**  Section OverHead, including frame synchronization bytes, network management information, etc.

**POH**  Path OverHead, function similar to SOH

**VC**  Virtual Container, “floating” within a TU / AU

**AU**  Administrative Unit = fixed payload + pointer(s)

**TU**  Tributary Unit, function similar to AU

- Tributaries (e.g., 2.048 Mbit/s PDH) are mapped into a VC either synchronously or asynchronously
- Several TU:s are multiplexed into a VC-4(3) via TUG:s
- VC:s are aligned to a TU / AU (using pointer processing)
Multiplexing of TU-12 into VC-4

Any TU-12 can be allocated a number in the form K, L, M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M designates the TU-12 number (1 to 3). The location of the 4 columns in the VC-4 occupied by TU-12 (K, L, M) is given by the formula:


\[(X = \text{column number} = 1 \ldots 4)\]

Thus TU-12(1, 1, 1) resides in columns 10, 73, 136, and 199 of the VC-4, and TU-12(3, 7, 3) resides in columns 72, 135, 198 and 261 of the VC-4.
Byte synchronous mapping of 2048 kbit/s

(1) Mapping of a 2048 kbit/s tributary into a VC-12
(2) Mapping of $31 \times 64$ kbit/s tributaries into a VC-12

The bytes V5, J2, N2 and K4 are allocated to the VC-12 POH. The V5 byte is the first byte of the multiframe and its position is indicated by the TU-12 pointer.
Asynchronous mapping of 2048 kbit/s

A 2048 kbit/s signal can also be mapped *asynchronously* into a VC-12 virtual container.

In this case, in addition to the VC-1 POH, the VC-12 consists of 1023 data bits, six justification control bits, **two justification opportunity bits**, eight overhead communication channel bits, fixed stuff bits (R), and O bits reserved for future overhead communication purposes.

Asynchronous mapping is used when the 2048 kbit/s signal is not synchronized with the VC-12 frame.
No pointer processing during transmission!

**Pointer processing**
- Assembly of STM-1 frame
- STM-1 cross-connect
- STM-1 – STM-4 multiplexing
- STM-4 cross-connect
- STM-4 cross-connect
- STM-4 – STM-1 demultiplexing
- Disassembly of STM-1 frame

**Pointer processing**
Retrieval of 2 Mb/s signal

1. Byte synchronization of STM-1
2. Read pointer of VC-4 (location of first byte of VC-4)
3. Locate required TUG-3, TUG-2, and TU-12 (fixed byte positions, therefore synchronous 1 : 63 demultiplexing)
4. Read pointer of VC-12 in TU-12 frame (location of first byte of VC-12)
5. If 2 Mb/s signal is mapped into VC-12 synchronously: simple byte demultiplexing
   6. If 2 Mb/s signal is mapped into VC-12 asynchronously: clock inhibit, elastic buffer, and PLL as in PDH case